UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,707	12/27/2001	Joseph Horanzy	87264.2600	9258

30734 7590 08/04/2005

BAKER & HOSTETLER LLP
WASHINGTON SQUARE, SUITE 1100
1050 CONNECTICUT AVE. N.W.
WASHINGTON, DC 20036-5304

EXAMINER	
STOYNOV, STEFAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,707	HORANZY ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,7,9,11-13,15,16,20-26,28,29,31,32,34,36,37,39,40,42,43,45 and 47-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *52-56* is/are allowed.

6)☒ Claim(s) *1,3,4,6,7,9,11-13,15,16,20-26,28,29,31,32,34,36,37,39,40,42,43,45,47-51 and 57* is/are rejected.

7)☒ Claim(s) *58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the slave processor providing a clock signal to the synchronous random access memory must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1 and 47 are objected to because of the following informalities:

In claim 1, line 4, the word "the" must be changed to "a".

In claim 47, on line 2, a space is required between the words "port and "static".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 6, 7, 26, 31, 32, 37, 39, 42, 43, 50, and 51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "processor" in lines 1, 2, and 9. Further, the claim recites the limitations "first processor" and "second processor". Thus, it is unclear for which processor some of the method steps are applicable.

Similarly, claim 3 and claims 6 and 7, depending on claim 1 recite the limitations "processor" and "plurality of processors" which render the claims unclear.

Claim 26 recites the limitation "processor" in lines 1, 12, and 15. Further, the claim recites the limitations "master processor", "second microprocessor", "second processor", and "first processor". Thus, it is unclear for which processor some of the method steps are applicable.

Similarly, claims 31 and 32, depending on claim 26 recite the limitation "plurality of processors" which renders the claims unclear.

Claim 37 recites the limitation "processor" in lines 1, 2, 4, 5, 7, and 8. Further, the claim recites the limitation "master processor". Thus, it is unclear for which processor some of the method steps are applicable. In the same claim, in line 4, the word "the" must be changed to "a".

Similarly, claim 39 and claims 42 and 43, depending on claim 37 recite the limitations "processor" and "plurality of processors" which render the claims unclear.

Claim 50 recites the limitation "nonvolatile memory device" in line 4. Further, in lines 2 and 3, the claim recites a first and second volatile memory devices containing a first and second identity with the master processor storing the first and second identities in the first and second volatile memory devices (lines 6 and 7). Thus, it is unclear what is the purpose of the limitation "nonvolatile memory devices", and thus there is insufficient antecedent basis for this limitation in the claim.

Claim 51 is rejected on the same grounds as independent claim 50 upon which it depends.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3, 4, 6, 7, 9, 11-13, 15, 16, 20-23, 36, 37, 39, 40, 42, 43, 45, 47, 48, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson, U.S. Patent No. 5,898,869 in view of Raatz et al., U.S. Patent No. 5,546,355.

Re claims 1 and 37, Anderson discloses a method and mechanism for bootstrapping a processor from a volatile memory device connected to the processor, comprising the steps of:

bootstrapping a first processor from a flash device;

[Anderson does not specifically state bootstrapping a first processor from a flash device. However, Anderson discloses using flash memory for storing initial load (and reload) code (i.e. boot code) (column 2, lines 7-10). Anderson further discloses a host computer (including a processor) transferring the boot sequence into the dual-ported memory of a PCMCI card (having its own separate processor) (column 8, lines 7-10, Fig. 1). In order for the host processor to be able to initiate the boot code transfer, the host processor must be operational (i.e. must have completed its own boot process and executed the boot code from the

flash memory). Thus, Anderson discloses bootstrapping a first processor from a flash device.]

asserting reset lines of the second processor (column 2, lines 35 and 36, lines 42-45, column 5, lines 57-59, column 6, lines 5-7, Fig. 2);

loading boot code for the second processor from the flash device into the volatile memory device (column 2, lines 64-67, column 3, lines 1 and 2, column 4, lines 41-49, column 8, lines 7-10);

[Anderson does not specifically state loading the boot code for the second processor from the flash device. However, Anderson discloses using flash memory for storing initial load (and reload) code (i.e. boot code) (column 2, lines 7-10). In addition, Anderson discloses downloading the boot code into the dual-ported memory, and booting the second processor using that boot code (column 5, lines 33-35). Thus, the boot code for the second processor is loaded from the flash memory, and thus Anderson discloses loading the boot code for the second processor from the flash device.]

de-asserting the reset lines of the second processor (column 2, lines 36-38, lines 42-45, column 3, lines 1 and 2),

wherein the processor performs the bootstrap procedure using the boot code stored in the volatile memory device (column 2, lines 64-67, column 3, lines 1 and 2, column 4, lines 41-44, column 5, lines 33-35).

Anderson fails to disclose the volatile memory implemented with synchronous static random access memory.

Raatz teaches using synchronous SRAM as a high-speed cache in data processing systems (column 1, lines 16-18). In Raatz, the synchronous SRAM (vs. asynchronous SRAM) requires fewer external logic chips and allows for higher system speeds of operation (column 1, lines 20-24). Thus, the circuit design area is reduced and operation with higher clock frequencies is achieved.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the synchronous SRAM, as suggested by Raatz for the volatile memory disclosed by Anderson in order to implement the volatile memory with synchronous static random access memory. One of ordinary skill in the art would be motivated to do so in order to reduce the circuit design area and achieve operation with higher clock frequencies.

Re claims 3 and 39, Anderson further discloses the method and mechanism, wherein a complex programmable logic device generates the reset lines of the processor (column 5, lines 13-15, lines 51-54, lines 57-59, Fig. 2).

Re claims 4 and 40, Anderson further discloses the method and mechanism as per claims 3, and 37, wherein the reset lines are controlled by the first processor and handled by the complex programmable logic device (column 5, lines 33-67, Fig. 2).

Re claims 6 and 42, Anderson further discloses the method and mechanism, wherein a plurality of processors are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory device (column 6, lines 21-25, Fig. 1, SRAM 27).

Re claims 7 and 43, Anderson further discloses the method and mechanism as per claims 6 and 42, wherein the first processor provides identity to each of the plurality of processors by posting information through volatile memory (column 6, lines 16-25).

Re claims 9 and 45, Anderson further discloses the method and mechanism, wherein the volatile memory device is dual port random access memory (column 4, lines 41-45, Fig. 1).

Re claim 11, Anderson and Raatz disclose the method as per claim 1. In addition, Anderson discloses using a dual-ported RAM (column 4, lines 44 and 45); Raatz teaches using synchronous SRAM for volatile memory (e.g. cache) (column 1, lines 16-18). Thus Anderson and Raatz disclose the volatile memory device is asynchronous dual port static random access memory.

Re claim 13, Anderson and Raatz disclose a system with all claim limitations as per claims 1, 6, and 7 addressed previously.

Re claim 15, Anderson further discloses the system, wherein the logic device is a complex programmable logic device (column 5, lines 51-54).

Re claim 16, Anderson does not specifically address implementing the logic device with a field programmable gate array. The examiner takes Official Notice that implementing logic devices with field programmable gate arrays (FPGAs) is well known. Using FPGAs allows in a flexible way to implement a wide variety of different logic functions. Accordingly, it would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to implement the logic device with a field programmable gate array.

Re claim 20, Anderson further discloses the system, wherein the volatile memory devices are static random access memories (column 4, lines 60-64, Fig. 1, SRAM 27).

Re claim 21, Anderson further discloses the system, wherein the volatile memory devices are dual port random access memory (column 4, lines 44 and 45).

Re claim 22, Raatz further teaches the system, wherein the volatile memory device is a synchronous static random access memory (column 1, lines 16-18).

Re claims 12, 23, 36, and 47, Anderson does not specifically state the synchronous static random access memory has a discontinuous clock through the bootstrapping procedure. However, Anderson discloses inserting and powering up the PCMCI card (column 7, lines 38-40, Fig. 5) after which the process of downloading the boot code to the dual-ported RAM is initiated as described previously. Thus, in the time period immediately following the power up the processor internal to the PCMCI card does not supply clock to the memory, and thus Anderson discloses the synchronous static random access memory has a discontinuous clock through the bootstrapping procedure.

Re claim 48, Anderson and Raatz disclose a computing system with all claim limitations as per claims 1 and 13 addressed previously.

Re claim 57, Anderson and Raatz disclose a computing system with all claim limitations as per claims 1 and 13 addressed previously. In addition, Anderson further discloses a data bus (Fig. 1, 21, 25, 26).

Claims 24-26, 28, 29, 31, 32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson, U.S. Patent No. 5,898,869 in view of Raatz et al., U.S. Patent No. 5,546,355, and further in view of Von Ahnen et al., U.S. Patent No. 6,400,717.

Re claim 24, Anderson and Raatz disclose the system as per claim 13. In addition Anderson discloses a plurality of slave flash devices each connected to one of the slave processors (column 6, lines 21-25, Fig. 1, FLASH 29).

Anderson and Raatz fail to disclose the slave flash devices having boot code for the slave processors, wherein the master processor determines whether to bootstrap the slave processors using a boot code in the slave flash devices or the boot code in the volatile memory devices.

Von Ahnen teaches selecting the boot mode for a slave processor (and booting the slave processor from either a ROM or a RAM associated with the slave processor), the mode selection controlled by a master processor (column 6, lines 8-12, lines 27-44, FIG. 2). Von Ahnen further teaches the slave processor's ROM containing a self-test program to boot the slave processor in test mode (column 6, line3 17 and 18). In Von Ahnen, the above-mentioned system and method allow for the master processor to direct the slave processor operation such that when booted in test mode, the slave processor validates itself, and when booted in system mode, the slave processor processes data received from the master processor (column 2, lines 63-67, column 3, lines 1-4). Thus, the slave processor could be tested and debugged, and validate its own

operation without using processing resources from the master processor (column 2, lines 43-53).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the ROM associated with a slave processor containing a self-test program booting the slave processor into test mode and the method for selectively booting into either the slave's ROM or RAM, as suggested by Von Ahnen with the system disclosed by Anderson and Raatz in order to implement the slave flash devices having boot code for the slave processors, wherein the master processor determines whether to bootstrap the slave processors using a boot code in the slave flash devices or the boot code in the volatile memory devices. One of ordinary skill in the art would be motivated to do so in order to provide means for self-testing and debugging of a slave processor without using processing resources from the master processor.

Re claim 25, Von Ahnen further teaches the system as per claim 24, wherein the master processor sets a command register in the logic device to configure logic units for the selected bootstrap procedure (column 6, lines 51-55).

Re claim 26, Anderson, Raatz and Von Ahnen disclose a method with all claim limitations as per claims 1, 13, 24, and 25 addressed previously.

Re claim 28, Anderson further discloses the method, wherein a complex programmable logic device generates the reset lines of the second processor (column 5, lines 13-15, lines 51-54, lines 57-59, Fig. 2).

Re claim 29, Anderson further discloses the method as per claim 28, wherein the reset lines are controlled by the master processor (column 5, lines 33-67, Fig. 2).

Re claim 31, Anderson further discloses the method, wherein a plurality of processors are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory device (column 6, lines 21-25, Fig. 1, SRAM 27).

Re claim 32, Anderson further discloses the method as per claim 31, wherein the master processor provides identity to each of the processors by posting information through the volatile memory devices (column 6, lines 16-25).

Re claim 34, Anderson further discloses the method, wherein the volatile memory is dual port random access memory (column 4, lines 44 and 45).

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson, U.S. Patent No. 5,898,869 in view of Raatz et al., U.S. Patent No. 5,546,355, and further in view of Ishinabe et al., U.S. Patent No. 5,572,468.

Re claim 49, Anderson and Raatz disclose a computing system with all claim limitations as per claims 1 and 13. In addition, Anderson discloses a data bus providing data communications between the synchronous random access memory and the slave processor (column 4, lines 60-64, Fig. 1, 25, 26). Anderson does not specifically state a slave processor providing clock signal to the synchronous random access memory. However, Anderson discloses the PCMCI card processor (slave processor) communicating over a data bus with the

SRAM and ROM local for that same card (column 5, lines 10-12, Fig. 1). This interoperation is controlled by a clock signal, thus Anderson discloses the slave processor providing clock signal to the synchronous random access memory.

Anderson and Raatz fail to disclose a pulldown resister network on the data bus.

Ishinabe teaches connecting a pulldown resistor to a data bus interconnecting a dynamic memory with a memory readout circuit (column 1, lines 41-44). In Ishinabe, the pulldown resistor is used to prevent the data bus from taking an uncertain level value while in high impedance state (column 1, lines 44-47), thus ensuring reliable data transfers.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the pulldown resistor connected to the memory bus, as suggested by Ishinabe for the computing system disclosed by Anderson and Raatz in order to implement a pulldown resister network on the data bus. One of ordinary skill in the art would be motivated to do so in order to ensure reliable data transfers.

Allowable Subject Matter

Claims 50 and 51 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 52-56 are allowed.

Claim 58 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 50, the prior art fails to disclose or suggest, alone or in combination "a master processor storing identity in the volatile memories of a plurality of slave processors, each slave processor obtaining the identity from its own volatile memory".

Re claim 52, the prior art fails to disclose or suggest, alone or in combination "submitting no-op commands to the processor until the processor provides a reliable clock signal".

Re claim 58, the prior art fails to disclose or suggest, alone or in combination "a pulldown resistor network on the data bus ensuring that the slave processor receives no-op instructions over the data bus during periods of clock instability".

Response to Arguments

Applicant's arguments with respect to claims 1, 3, 4, 6, 7, 9, 11-13, 15, 16, 20-26, 28, 29, 31, 32, 34, 36, 37, 39, 40, 42, 43, 45, and 47 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

SS